UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/558,090	11/23/2005	Jose de Jesus Pineda De Gyvez	NL 030629	3397

65913 7590 08/24/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
08/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/558,090	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 16 July 2007 has been entered.

Response to Arguments

Applicant's arguments filed on 16 July 2007 have been fully considered but they are not persuasive.

Applicant has amended the independent claims to recite circuitry for providing analog control signals in response to monitoring the input and output signals of sequential logic elements, and means for producing a combined analog control signal from a plurality of individual analog control signals [independent claims 1 and 6].

The examiner does not find applicant's amendments to be sufficient to define over the prior art. To the extent that all digital signals are inherently analog, the teachings of Elappuparackal sufficiently anticipate the claimed invention. Specifically, while the examiner recognizes that the monitoring circuitry of Elappuparackal is comprised of digital logic gates, the signals output by the gates are inherently analog in that the signals are comprised of voltage and/or currents that change continuously over a period of time. A digital value for an analog signal is merely an abstraction of the voltage/current level of the signal, wherein a value of 1 or 0 is assigned to an analog voltage/current depending on its relation to a predetermined high/low threshold.

Additionally, the examiner wishes to note that it is unclear what analog control signals are being claimed by the applicant. Applicant's disclosure teaches that the monitoring circuitry is comprised of logic gates and/or transistors that output *digital* values for the control signal [Fig. 2-4, tables 1 and 2, pp. 7-8 of originally filed specification].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Elappuparackal, U.S. Patent No. 6,822,478 B2.

Regarding claim 1, Elappuparackal teaches an electronic circuit [Fig. 5] comprising:

a plurality of sequential logic elements [flip-flops 40-43] comprising:

at least one clock terminal for receiving a clock signal [clk];

at least one input terminal for receiving an input signal [Din(0...3)];

at least one output terminal for providing an output signal [Q];

circuitry for respective ones of the plurality of sequential logic elements for monitoring respective ones of said input and output signals [XOR gates 140-143] to provide respective control signals in response thereto [outputs of XOR gates 140-143];

and means for combining said respective control signals to form a combined control signal [OR gates 45-47, clock logic 102] and controlling a power consumption of the electronic circuit in response to said combined control signal [GCLK, col. 2, lines 1-9, col. 3, lines 40-46, col. 4, lines 5-11, col. 5, line 39 to col. 6, line 21].

Regarding claim 2, Elappuparackal teaches that the circuit is controlled at a rate determined by the clock signal.

Regarding claim 5, Elappuparackal teaches an apparatus that includes the circuit [col. 8, lines 29-37].

Regarding claim 6, Elappuparackal teaches the circuit of claim 1, and also the method implemented by the claimed circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elappuparackal in view of Gasztonyi, U.S. Patent No. 5,339,445.

Regarding claims 3 and 4, Elappuparackal discloses the circuit of claim 1, but does not teach the provision of information related to future power consumption based on past logical events.

Gasztonyi discloses a computer system that compiles a history of the utilization of various assets within the computer system. Based on the history, the system predictively activates/deactivates the assets [col. 3, line 64 to col. 4, line 9].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Elappuparackal and Gasztonyi by applying the predictive power controlling method of Gasztonyi in the system of Elappuparackal. Both Elappuparackal and Gasztonyi are concerned with reducing power consumption in computer system. Elappuparackal teaches that the circuit may be implemented in the context of a microprocessor-based system [col. 6, lines 51-61]. The teachings of the Gasztonyi would improve the microprocessor-based system of Elappuparackal by allowing predictive control of the power supplying function, thus reducing power consumption, while at the same time preventing waiting time for the assets to be fully powered [Gasztonyi, col. 4, lines 6-9].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
U.S. Patent and Trademark Office
571-272-7181
ji.bae@uspto.gov

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100